CLAIMS

I claim:

1    1.    An apparatus comprising:

2         a first clock domain to operate at a first clock frequency;

3         a second clock domain to operate at a second clock frequency; and

4         an interface disposed between the first and second clock domains to control

5    timing of data transfer from one of the first or second clock domains to other of the first

6    or second clock domains, the interface to allow for a frequency ratio between the first and

7    second clock domains which is not an integer ratio.

1    2.    The apparatus of claim 1, wherein the interface is made programmable to allow

2    selection of different frequency ratios to be selected between the first and second clock

3    domains.

1    3.    The apparatus of claim 1, wherein the interface is to allow for a granularity of

2    0.25 in the frequency ratio between the first and second clock domains.

1    4.    The apparatus of claim 1, wherein the first clock domain is a bus domain and the

2    second domain is a circuit operably coupled to the bus domain.

1    5.    The apparatus of claim 1, wherein the interface to allow for data transfer in both

2    directions in which first domain operates at a faster frequency than the second domain.

1    6.    The apparatus of claim 1, wherein the interface includes a control circuit to set the

2    frequency ratio and at least one latching circuit to latch data through the interface from

3    one clock domain to the other clock domain.

1    7.    The apparatus of claim 6 further including a plurality of latching circuits, in which

2    separate latching circuits are to be used to transfer data in a particular direction between

3    the first and second clock domains.

1    8.    The apparatus of claim 7, wherein the control circuit of the interface further

2    includes a first and second ratio generators in which the first ratio generator is to be used

3    to generate control signals to the latching circuits, if the ratio difference is below a

4    particular ratio and the second ratio generator is to be used to generate control signals to

5    the latching circuits if the ratio difference is equal to or above the particular ratio.

1    9.    An integrated circuit comprising:

2         a first clock domain to operate at a first clock frequency;

3  a second clock domain to operate at a second clock frequency; and

4  an interface disposed between the first and second clock domains to control

5 timing of data transfer in both directions between the first clock domain and the second

6 clock domain, the interface to allow for a frequency ratio between the first and second

7 clock domains which is not an integer ratio.

1 10. The integrated circuit of claim 9, wherein the first domain is a bus domain and the

2 second domain is operably coupled to the bus domain to transfer data to and from the bus

3 domain.

1 11. The integrated circuit of claim 10, wherein the first and second domains are

2 synchronized from a same clock source, but in which the first domain operates at a faster

3 clock frequency than the second domain.

1 12. The integrated circuit of claim 11, wherein the interface is to allow for a

2 frequency ratio of N:4, where N is an integer, to have a granularity 0.25 for the frequency

3 ratio between the first and second clock domains.

1 13. The integrated circuit of claim 11, further including a plurality of additional clock

2 domains operably coupled to the bus domain and in which a separate interface is disposed

3 between the bus domain and the additional domains, the interfaces made programmable

4 to allow selection of different frequency ratios to be selected between the bus domain and

5 the additional domains.

1 14. The integrated circuit of claim 13, wherein individual interfaces include a control

2 circuit to set the frequency ratio and at least one latching circuit to latch data through the

3 interface between the bus domain and respective domain operably coupled to the bus

4 domain.

1 15. A method comprising:

2  generating a first clock signal having a first frequency to a first clock domain;

3  generating a second clock signal having a second clock frequency to a second

4 clock domain, a ratio between the first clock frequency to the second clock frequency

5 being a non-integer ratio; and

6  using an interface disposed between the first and second clock domains to control

7 timing of data transfer from the first clock domain to the second clock domain, the

8    interface made programmable to set a particular frequency ratio based on ratio of the first

9    clock frequency to the second clock frequency.

1    16.    The method of claim 15, wherein the first domain is a bus domain and the second

2    domain is operably coupled to the bus domain in transferring data to and from the bus

3    domain, the bus domain operating at a faster clock frequency.

1    17.    The method of claim 16, wherein the ration between the first and second clock

2    frequencies allows for a frequency ratio of N:4, where N is an integer, to have a

3    granularity 0.25 for the frequency ratio between the first and second clock domains.

1    18.    The method of claim 16, further including using a plurality of additional clock

2    domains operably coupled to the bus domain and in which a separate interface is used

3    between the bus domain and the additional domains, the interfaces made programmable

4    to allow selection of different frequency ratios to be selected between the bus domain and

5    the additional domains.

1    19.    The method of claim 16, further including latching data from the bus domain to

2    the second domain by counting a difference in the clock pulses based on the particular

3    frequency ratio and skipping certain ones of excess clock pulses to have a one-to-one data

4    transfer timing between the two clock domains.

1    20.    The method of claim 16, further including latching data from the bus domain to

2    the second domain by counting a difference in the edges based on the particular

3    frequency ratio and skipping certain ones of excess clock edges to have a one-to-one data

4    transfer timing between the two clock domains.